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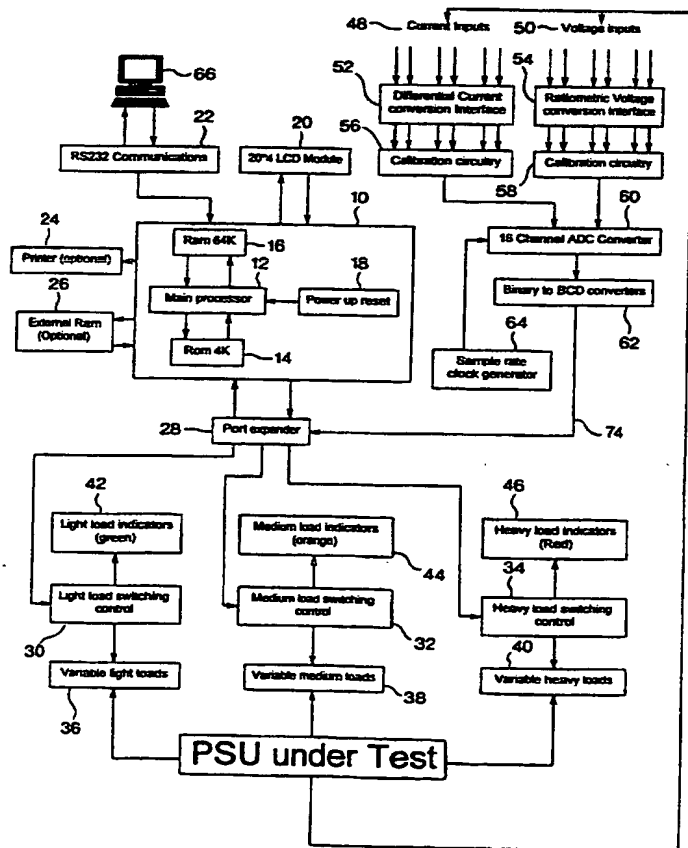
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(54) Title: POWER SUPPLY ANALYSER



(57) Abstract: A power supply analyser is designed to test a multiple-output power supply, such as those which power automatic teller machines (ATM's). A set of variable loads are provided for each output of the power supply, with current and voltage sensors for monitoring the performance of the power supply when supplying the loads. A control circuit varies the magnitude of each load according to a predetermined scheme, increasing the loads from light to heavy, while a monitoring circuit monitors the outputs of the current and voltage sensors and assesses the performance of the power supply.

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POWER SUPPLY ANALYSER

BACKGROUND OF THE INVENTION

THIS invention relates to a power supply analyser which can be used to monitor the performance of electronic power supplies.

Sophisticated electronic and electromechanical equipment may have multiple power supplies which operate at different output voltages for operating the various electronic and electromechanical circuits of the equipment.

Traditionally, each output of the power supply is checked by measuring its output voltage, preferably *in situ*. Apart from being somewhat time consuming, such measurements provide relatively little information.

It is an object of the invention to provide a power supply analyser which automatically tests multiple outputs of a power supply.

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SUMMARY OF THE INVENTION

According to the invention a power supply analyser comprises:

a plurality of variable loads connectable to respective ones of a plurality of outputs of a multiple-output power supply;

at least one current sensor arranged to measure the current in each load and to generate respective current signals corresponding to the measured currents;

at least one voltage sensor arranged to measure the output voltage at each output and to generate respective voltage signals corresponding to the measured voltages;

a control circuit arranged to vary the magnitude of each load according to predetermined criteria; and

a monitoring circuit responsive to the current and voltage signals to monitor the behaviour of the power supply while each output thereof is subjected to a varying load.

The control circuit is preferably a microprocessor based circuit arranged to select one of a plurality of different loads for connection to each output.

For example, a light, medium and heavy load may be provided for each output, the actual magnitude of each load being related to the load rating of the respective output.

The variable loads may be supplied in the form of one or more load modules which are removably connectable to the analyser.

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Preferably, the control circuit is arranged to apply lighter loads to each output before applying heavier loads thereto.

The control circuit may further be arranged to apply loads to respective outputs individually, before applying loads to a plurality of outputs simultaneously.

The monitoring circuit preferably includes at least one analogue to digital converter, and a software-controlled processor arranged to compare output waveforms of each output with stored reference values or waveforms.

The monitoring circuit may further be arranged to store data from each measurement cycle for comparison with subsequent measurements.

BRIEF DESCRIPTION OF THE DRAWINGS

- Figure 1** is a schematic block diagram of a power supply analyser according to the invention;
- Figure 2** is a schematic diagram illustrating the functions carried out by the analyser of Figure 1;
- Figure 3** is a simplified flowchart illustrating the main functions of the analyser; and
- Figure 4** is a simplified schematic block diagram of the load control scheme of the analyser.

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DESCRIPTION OF AN EMBODIMENT

Figure 1 shows the main electronic components of a power supply analyser according to the invention. The analyser is based on a microprocessor 10 which includes a main processor or CPU 12, read only memory (ROM) 14 and random access memory (RAM) 16 as well as a power-up reset circuit 18. Associated with the microprocessor 10 are a twenty character by four line liquid crystal display (LCD) module 20, an RS232 communications interface 22, an optional printer 24, optional external RAM 26, and a port expander interface 28.

Connected to the microprocessor 10 via the port expander interface 28 are three load control circuits 30, 32 and 34, which are arranged to control a set of variable light, medium and heavy loads 36, 38 and 40, respectively. Associated with each control circuit 30, 32 and 34 is an illuminated load indicator 42, 44 or 46. The indicators include green, orange and red LED's respectively, to indicate to an operator that a light, medium or heavy load has been selected.

A typical power supply intended to be monitored by the power supply analyser has six separate outputs, so that the analyser has a set of six current inputs 48 and six voltage inputs 50 for monitoring the current and output voltage of each output. Each current input is measured by a differential current conversion interface 52, while each voltage input is measured by a radiometric voltage conversion interface 54. The outputs of the respective interfaces 52 and 54 are fed to calibration circuits 56 and 58, the outputs of which are fed to a sixteen channel analogue to digital converter 60. A sample rate clock generator 64 determines the sampling rate of the analogue to digital converter.

The digital output of the analogue to digital converter 60 is fed to a binary to binary coded decimal (BCD) converter 62, the outputs of which is fed to the

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microprocessor 10 via the port expander interface 28. Thus, the microprocessor is fed with the measured current and voltage output values for each output of the power supply simultaneously.

As best seen in Figure 4, an output 66 of a power supply under test has its output current and voltage measured by the respective current and voltage conversion interfaces 52 and 54. The light, medium and heavy loads 36, 38 and 40 are controlled by relay switches 68 and 70 (the light load 36 is connected directly to the power supply output and therefore does not have its own switch). The relay switches 68 and 70 are controlled via an 8 bit bus 52, by the microprocessor 10. The data output from the current and voltage conversion interfaces 52 and 54 is fed back to the microprocessor (after A to D conversion and binary to BCD conversion) via an 8 or 12 bit data bus 74.

The operation of the power supply analyser is shown graphically in the flowchart of Figure 3.

The operation of the analyser can be summarised as follows. Firstly, a relatively light load is applied to each individual power supply output. Each output is monitored by comparing the output waveform with a stored reference waveform (or one or more reference values) for deviations from the expected performance. Assuming that the monitored performance is within an acceptable range, the load on each output is increased and the process repeated until the maximum load for each output is reached.

The data from the above procedure is output to a PC 66 via the RS232 interface 22 which is used to generate graphs or other graphic displays of the output waveforms for comparison and analysis. Apart from this, the monitored values for output current and voltage are displayed on the LCD module 20. In the case where a PC 66 is not available, the data from a set of measurements can be stored in the RAM 16 or 26 for later downloading.

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Because the connection of the loads to the power supply under test is controlled by the microprocessor 10, the load switching scheme can be changed by the user as required. In the prototype system, the software for the microprocessor was written so that the analyser operates in the sequence set out below.

The analyser starts by applying one light load on a first supply rail (say, the -5V output). Current and voltage measurements are taken. The load is then removed and applied to the next supply rail (say, +5V) and measurements are taken again. Next, two light loads are applied, one to the -5V rail and one to the +5V rail and measurements are again taken. In the next step, both loads are removed and a light load is applied to the next supply rail (say, -12V) and measurements are taken. The procedure for the -5V and +5V rails is then repeated, at the end of which three loads are applied to the three outputs (ie. -5V, +5V and -12V). All the loads are removed and the sequence is repeated for the fourth output (say, the +12V rail). And the process is repeated until all supply rails have been tested in combination and individually.

In an average power supply having six different voltage rails, this will result in sixty three different loading conditions for each type of load. The time for which each load is connected is software controlled and can be set by the user.

It will be appreciated that the loads can be purely resistive, or can combine resistive, capacitive and/or inductive components. Technically, the loads will comprise series resistors of a value less than 0.1 Ω .

The power supply analyser can be built as a portable unit for use in the field, or can, for example, be combined with an adapter which allows it to be connected sequentially to a number of power supplies, typically for production testing.

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Power supplies under test do not have to be the same make or model as long as the necessary connections are available.

In the prototype system, the power supply analyser was able to take over eighteen thousand samples simultaneously in just under one hour. Multiplied by the number of loading conditions that can be applied, a large amount of data can be obtained from the power supply under test.

In order to compare the "electronic signatures" obtained from a power supply, graphs are plotted for the six different measured voltages and currents for each power supply output. Corresponding graphs can also be plotted for the input AC current and voltage. Input and output power can then also be calculated over a period of time, allowing the efficiency of the power supply to be determined and compared with a reference value.

For a given power supply, the user enters 24 different threshold levels, which can be obtained from the power supply manufacturer or determined empirically. After a test routine, the following data will typically be provided to the user:

Vaverage = xx (for 6 readings)

Vpeak = xx (for 6 readings)

Vmin = xx (for 6 readings)

Vmax = xx (for 6 readings)

Iave = xx (for 6 readings)

Ipeak = xx (for 6 readings)

Imin = xx (for 6 readings)

Imax = xx (for six readings)

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Number of times upper threshold level was exceeded = xx (for 12 readings)

Number of times lower threshold level was exceeded = xx (for 12 readings)

Ave power out = xx

Ave power in = xx

Efficiency = xx

It will be appreciated that the abovementioned list of output figures will provide about 75 figures to the user, which a skilled user can interpret relatively easily. The data for each power supply tested is stored and allows the user to build up a data base for comparison in future tests.

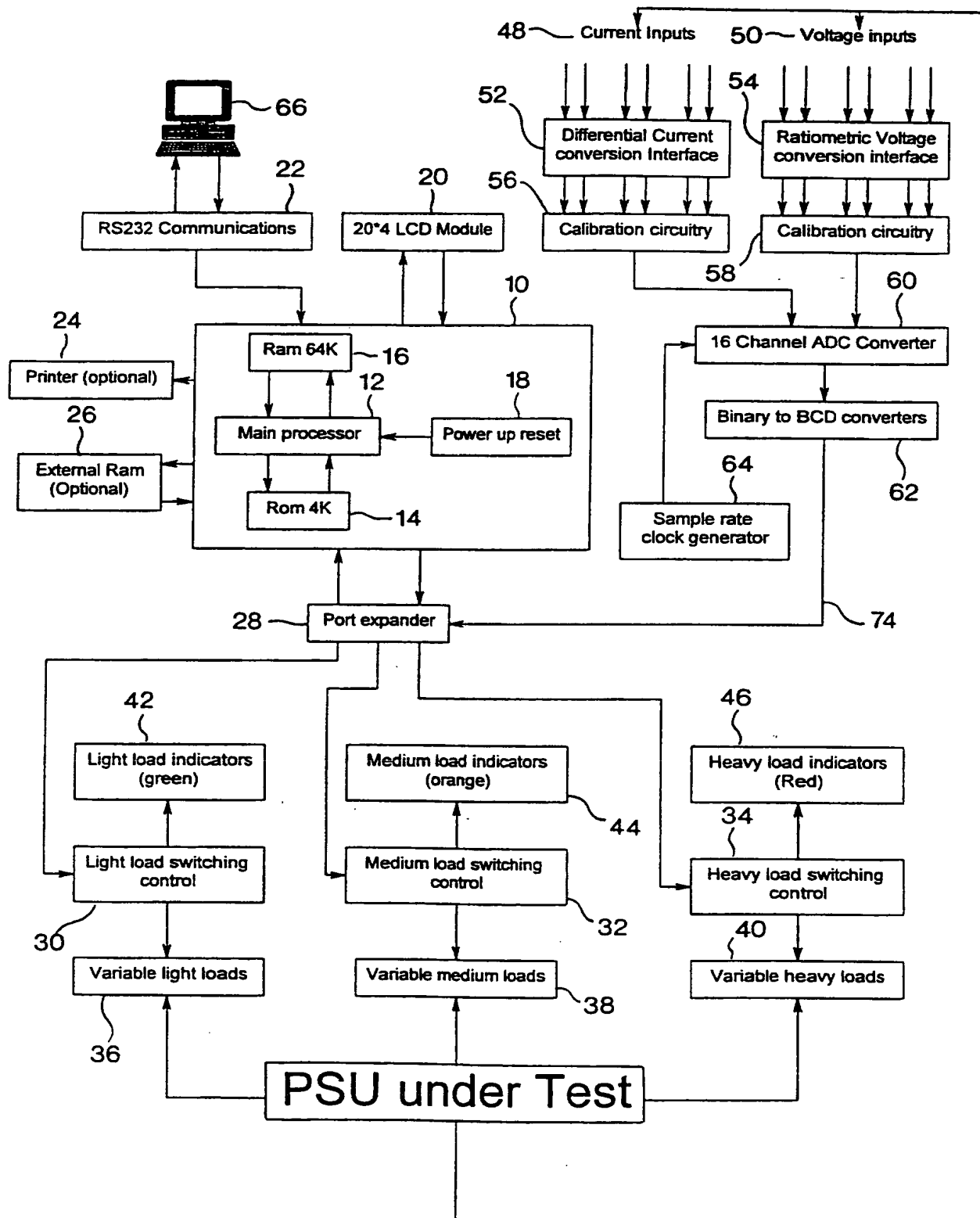
It will be appreciated that the exact parameters tested can be varied, as can the number of measurements, the number and nature of the variable loads, and so on.

CLAIMS

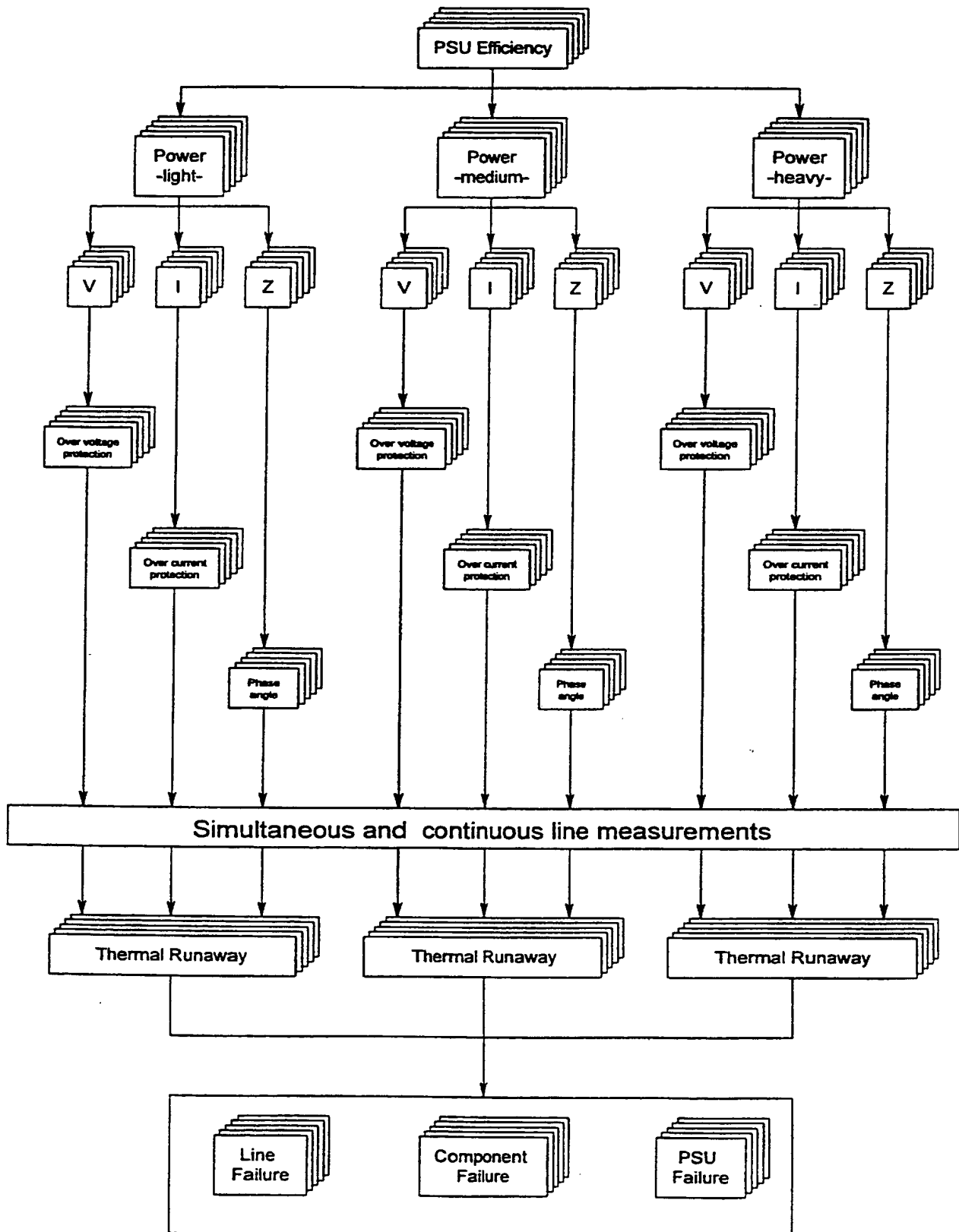
1. A power supply analyser comprising:
 - a plurality of variable loads connectable to respective ones of a plurality of outputs of a multiple-output power supply;
 - at least one current sensor arranged to measure the current in each load and to generate respective current signals corresponding to the measured currents;
 - at least one voltage sensor arranged to measure the output voltage at each output and to generate respective voltage signals corresponding to the measured voltages;
 - a control circuit arranged to vary the magnitude of each load according to predetermined criteria; and
 - a monitoring circuit responsive to the current and voltage signals to monitor the behaviour of the power supply while each output thereof is subjected to a varying load.
2. A power supply analyser according to claim 1 wherein the control circuit is a microprocessor based circuit arranged to select one of a plurality of different loads for connection to each output.
3. A power supply analyser according to claim 2 wherein a light load, a medium load and a heavy load are provided for each output, the actual magnitude of each load being related to the load rating of the respective output.

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4. A power supply analyser according to any one of claims 1 to 3 wherein the variable loads take the form of at least one load module which is removably connectable to the analyser.
5. A power supply analyser according to any one of claims 1 to 4 wherein the control circuit is arranged to apply lighter loads to each output before applying heavier loads thereto.
6. A power supply analyser according to claim 5 wherein the control circuit is further arranged to apply loads to respective outputs individually, before applying loads to a plurality of outputs simultaneously.
7. A power supply analyser according to any one of claims 1 to 6 wherein the monitoring circuit includes at least one analogue to digital converter, and a software-controlled processor arranged to compare output waveforms of each output with stored reference values or waveforms.
8. A power supply analyser according to claim 7 wherein the monitoring circuit is arranged to store data from each measurement cycle for comparison with subsequent measurements.

FIG 1

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FIG 2

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Fig 3

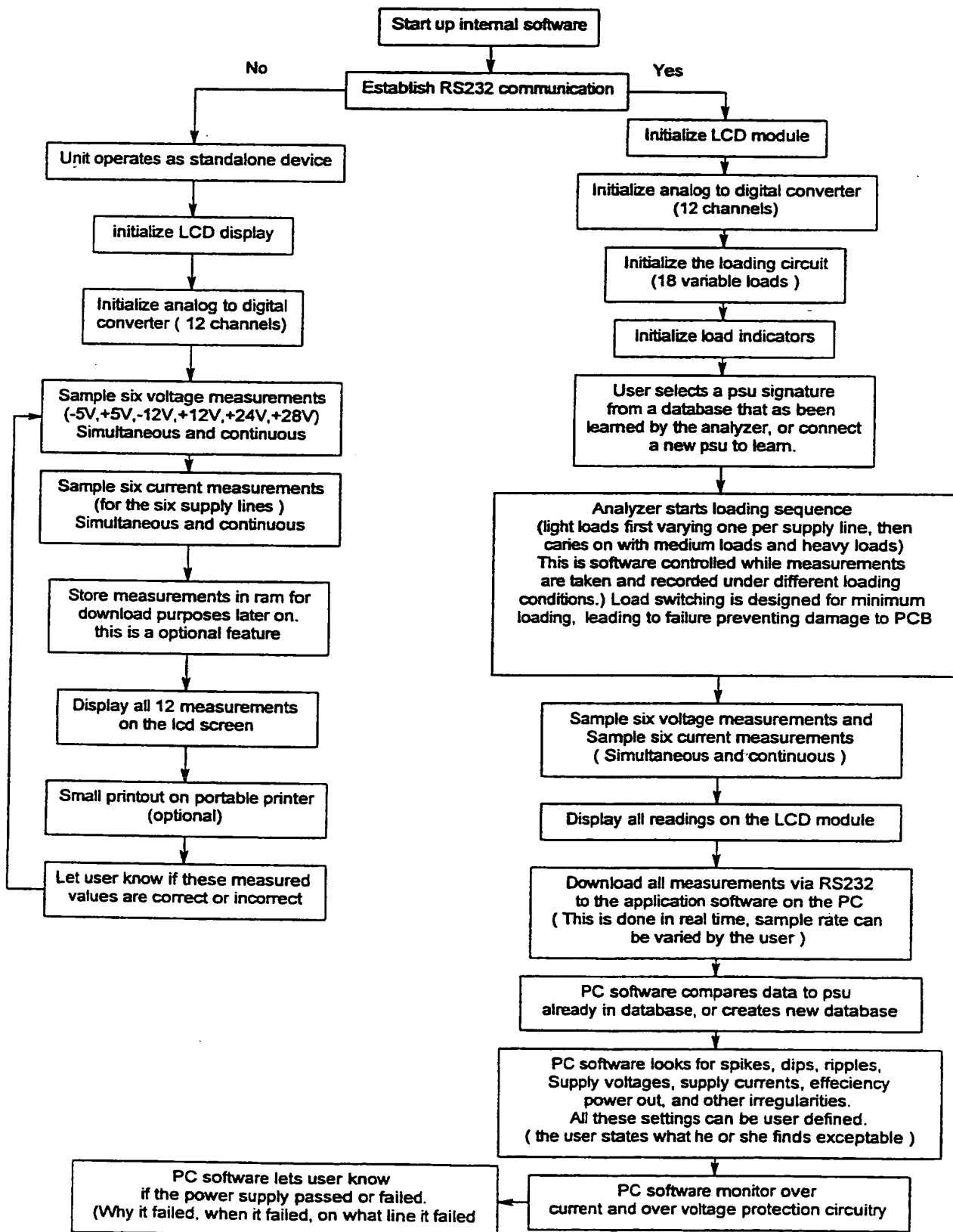
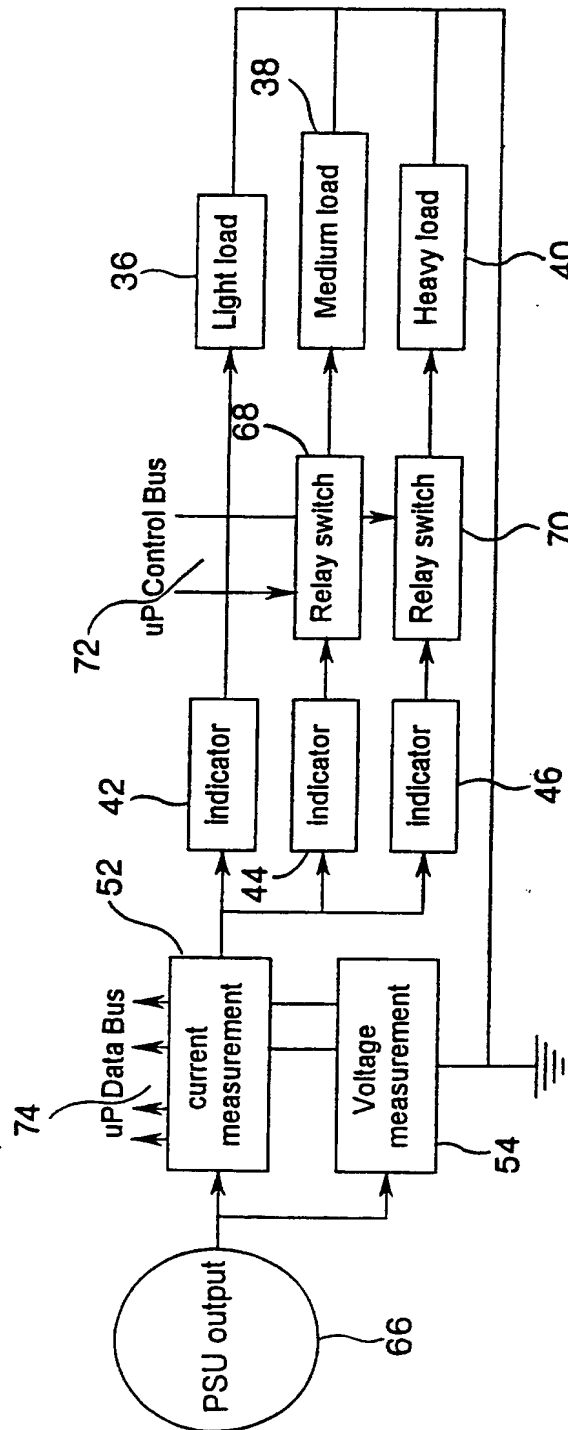


FIG. 4

INTERNATIONAL SEARCH REPORT

Internatio Application No

PCT/Ib 01/00080

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R31/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 037 156 A (GOUJON ROGER HUBERT ET AL) 19 July 1977 (1977-07-19) claims 1-3,6-9 figure 1	1-3,8
A	US 5 497 332 A (ALLEN CHARLES R ET AL) 5 March 1996 (1996-03-05) column 2, line 59 -column 3, line 4	1,7

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/IB 01/00080

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4037156 A	19-07-1977	FR 2310024 A	26-11-1976
		DE 2619289 A	11-11-1976
		GB 1521373 A	16-08-1978
		IT 1058705 B	10-05-1982
		JP 1247799 C	16-01-1985
		JP 51134029 A	20-11-1976
		JP 59025464 B	18-06-1984
US 5497332 A	05-03-1996	NONE	

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